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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,080	10/22/2003	Barry E. Burke	MIT8431L	9280

7590 06/02/2006

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EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/691,080	BURKE ET AL.	
	Examiner	Art Unit	
	Chuong A. Luu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/6/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 18-20* is/are rejected.

7)☒ Claim(s) *16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 1-6, 12, 14-15 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hynecek (U.S.5,972,733) in view of Matsuoka et al. (U.S.6,130,449).

Hynecek discloses a method making a virtual phase charge coupled device with

(1); (18); (19); (20) forming an electrically conducting charge transfer channel (24) in a semiconductor substrate (22);

forming an electrically insulating layer (26) on a surface of the substrate (22);

forming a layer of gate electrode material on the insulating layer (26) (see Figure 1);

forming on the gate material layer a first patterned masking layer (70) having apertures that expose regions of the underlying gate material layer that are to form gate electrodes (see Figure 1);

electrically doping the first-pattern-exposed regions of the gate material layer (24) (see column 2, lines 12-40);

etching the second-pattern-exposed regions of the gate material layer (see Figure 3);

(2) further comprising removal of the first patterned masking layer after electrically doping first-pattern-exposed regions of the gate material layer (see Figure 1);

(3) further comprising removal of the second patterned masking layer after etching second-pattern-exposed regions of the gate material layer (see Figure 1);

(4) wherein the first-pattern-exposed regions of the gate material layer are electrically doped before the second-pattern-exposed regions of the gate material layer are etched (see Figure 1);

(5) wherein electrically doping first-pattern-exposed regions of the gate material layer comprises ion implantation of a selected electrical dopant into the first-pattern-exposed regions of the gate material layer (see column 2, lines 12-40);

(6) wherein etching the second-pattern-exposed regions of the gate material layer comprises plasma etching the second-pattern-exposed regions of the gate material layer (see Figure 3);

(12) wherein forming an electrically insulating layer on a surface of the substrate comprises forming a layer of oxide on the substrate surface (see Figures and 3);

(14) wherein forming a layer of gate electrode material on the insulating layer comprises depositing a layer of polysilicon on the insulating layer (see Figures and 3);

(15) wherein forming a first patterned masking layer and forming a second patterned masking layer each comprise forming a layer of photoresist that is photolithoraphically patterned (see Figures and 3).

Hynecek teaches the above outlined features except for forming on the gate material layer a second patterned masking layer having apertures that expose regions of the underlying gate material layer that are to form gaps between gate electrodes. However, Matsuoka discloses a semiconductor device with **(1); (18); (19); (20).....** forming on the gate material layer a second patterned masking layer having apertures that expose regions of the underlying gate material layer that are to form gaps between gate electrodes (see Figures 7-8). Therefore, It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teachings of Hynecek and Matsuoka to fabricating a semiconductor device. Doing so would facilitate the manufacture of the semiconductor device and increase the speed of the semiconductor structure.

Claims 7-11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hynecek (U.S.5,972,733) in view of Matsuoka et al. (U.S.6,130,449) and Rhodes (U.S.4,742,016) and further in view of Erhardt (U.S. 5,114,833).

Hynecek and Matsuoka teach everything above except for heat treating the electrically doped gate electrodes. However, Rhodes discloses a semiconductor device with **(7)** further comprising heat treating the electrically-doped and etched gate electrode material layer to diffuse the electrical dopant through the gate material layer thickness (see column 5, lines 4-27); **(8)** wherein heat treating the electrically-doped and etched gate electrode material layer comprises annealing the gate material layer (see column 5, lines 4-27); **(9)** wherein heat treating the electrically-doped and etched gate electrode material layer comprises oxidation of the gate material layer (see column 5, lines 4-27); **(10)** wherein forming a first patterned masking layer and forming a second patterned masking layer each comprise forming a masking layer having a pattern the apertures of which are characterized by an extent accounting for lateral dopant diffusion during the heat treatment (see column 4, lines 20-57 and column 5, lines 4-27).

Hynecek, Matsuoka and Rhodes disclose the above outlined features except for wherein forming an electrically conducting charge transfer channel in a semiconductor substrate comprises ion implantation of a selected electrical dopant into a silicon substrate, the selected electrical dopant being of a conductivity type opposite that of the silicon substrate; wherein forming a layer of gate electrode material on the insulating layer comprises depositing a layer of amorphous silicon on the insulating layer. However, Erhardt discloses a charge-coupled-device with **(11)** wherein forming an

electrically conducting charge transfer channel in a semiconductor substrate comprises ion implantation of a selected electrical dopant into a silicon substrate, the selected electrical dopant being of a conductivity type opposite that of the silicon substrate (see column 2, lines 36-58. Figures 5-9); **(13)** wherein forming a layer of gate electrode material on the insulating layer comprises depositing a layer of amorphous silicon on the insulating layer; it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teachings of Hynecek, Matsuoka and Rhodes (accordance with the teaching of Erhardt), since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. Doing so would facilitate the manufacture of the semiconductor device and enhance the performance of the semiconductor device.

Allowable Subject Matter

Claims 16-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Patent Examiner
May 25, 2006